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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,462	05/11/2005	Daniel Chatroux	123886	5027
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EXAMINER				
MEMULA, SURESH				
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2825				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/534,462

**Applicant(s)**

CHATROUX ET AL.

**Examiner**

SURESH MEMULA

**Art Unit**

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 August 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 17-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 17-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This office action is a response to the RCE filed on 8/25/2008. After further consideration, the prior art rejections under the Tamura reference are withdrawn. However, this application is not in condition for allowance in view of the newly considered art detailed below. Claims 17-35 are pending, of which claims 31-35 are newly added.

#### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/25/2008 has been entered.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 17-29 and 31-35 are rejected under 35 U.S.C. 102(e)** as being anticipated by US Pub. No. 2003/0155963 to Huang (Hereinafter: Huang).

4. As to claim 17,  
an integrated circuit comprising at least a digital part comprising a plurality transistors connected to one another so as to form a plurality of functional elements (¶28),

the functional elements being grouped in subassemblies (FIG. 2: Subassembly 1: elements 218-219; Subassembly 2: elements 220-221) each comprising a first and a

second electrical supply terminal (FIG. 2: elements Vdd and GND) and a clock input (FIG. 2: input line elements 210/211 and 212/213 corresponding to transistors 218-221), the subassemblies being connected in series by their supply terminals to the terminals of a voltage supply source (FIG. 2: elements 218-221 are connected in series to Vdd and GND),

wherein a same clock signal is applied to the clock input of all subassemblies (FIG. 2: element CLK at input of element 223) by a device for shifting the levels of the clock signals (FIG. 2: elements 214-217 or 222-226),

wherein the subassemblies are formed in such a way that a same current flows through each of the subassemblies (FIG. 2: subassemblies 218-219 and 220-221 are connected in series, thus the current, at all times, is the same).

5. As to claim 18, wherein the clock inputs of at least two adjacent subassemblies are connected by a device for shifting the clock signal levels (FIG. 2: elements 214-217 or 223-226).
6. As to claim 19, wherein the clock input of an end subassembly is connected by an additional device for shifting the clock signal levels at the output of the clock circuit (FIG. 2: Subassembly 218-219 with corresponding elements 222, 214-215, 223-224; or Subassembly 220-221 with corresponding elements 216-217, 225-226).
7. As to claim 20, wherein the device for shifting the clock signal levels comprises at least one capacitor (FIG. 2: elements 214-217).
8. As to claim 21, wherein the device for shifting the clock signal levels comprises at least one transistor (¶21; FIG. 2: elements 223-226 or 218-222).
9. As to claim 22, wherein all the subassemblies are identical (FIG. 2: subassemblies 218-219 and 220-221 are both electrical components).
10. As to claim 23, wherein each of the subassemblies comprises a voltage limiting circuit connected between the first and the second electrical supply terminals (¶3, 19, 30-33; FIG. 2: elements 218-222).
11. As to claim 24, wherein the voltage limiting circuit comprises a diode (¶3, 19, 30-33).

12. As to claim 25, wherein the voltage limiting circuit comprises a transistor (FIG. 2: elements 218-222).
13. As to claim 26, wherein each subassembly comprises a decoupling capacitor connected between the first and second electrical supply terminals of the subassembly (FIG. 2: elements 214-217,  $C_{out}$ ).
14. As to claim 27, wherein the integrated circuit comprises electrical insulation between the subassemblies (¶3, 19, 30-33; FIG. 2: elements 218-222).
15. As to claim 28, wherein the means for electrical insulation between the different subassemblies are reverse biased diode junctions (¶3-5, 19, 30-33; FIG. 1-2: elements 218-222).
16. As to claim 29, wherein the means for electrical insulation between the different subassemblies are dielectric zones (¶3-5, 19, 30-33; FIG. 1-2: elements 218-222).
17. As to claim 31, wherein the subassemblies are at different electrical potentials (FIG. 2: Subassembly 218-219 is closer to a positive potential; Subassembly 220-221 is closer to a negative potential), wherein a potential difference between two end subassemblies is greater than a potential difference between terminals of each subassembly (FIG. 2, in example, at the Vdd end of subassembly 218-219 the potential is positive x, at the GND end of subassembly 220-221 the potential is zero; thus the difference of the ends is always x, and due to impedance is always greater than the individual potential at each subassembly.).
18. As to claim 32, wherein a voltage level of the clock signal applied to the clock input of each subassembly is adapted to voltages present at the first and second electrical supply terminals of the corresponding subassembly (FIG. 2: elements 222-226).
19. As to claim 33, wherein the same current flowing through the different subassemblies varies by less than 20% (FIG. 2: subassemblies 218-219 and 220-221 are connected in series, thus the current, at all times, is equivalent and therefore less than 20%).
20. As to claim 34, wherein the subassemblies are formed in such a way that, at all times in operation, the same current flows through each of the subassemblies (FIG. 2:

subassemblies 218-219 and 220-221 are connected in series, thus the current, at all times, is the same).

21. As to claim 35,

applying a same clock signal to a clock input of all subassemblies (FIG. 2: element CLK at input of element 223) via a device for shifting the levels of the clock signals (FIG. 2: elements 214-217 or 222-226),

the subassemblies being in a structure in which an IC comprises at least a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements (§128),

the functional elements being grouped in subassemblies each comprising a first and a second electrical supply terminal (FIG. 2: elements Vdd and GND) and a clock input (FIG. 2: input line elements 210/211 and 212/213 corresponding to transistors 218-221),

the subassemblies being connected in series by their supply terminals to the terminals of a voltage supply source (FIG. 2: elements 218-221 are connected in series to Vdd and GND),

wherein the subassemblies are formed in such a way that, at all times, the same current flows through each of the subassemblies (FIG. 2: subassemblies 218-219 and 220-221 are connected in series, thus the current, at all times, is the same).

***Claim Rejections - 35 USC § 103***

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. **Claim 30 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Huang in view of one or more of:

US Pub. No. 2004/0077151 to Bhattacharyya (Hereinafter: Bhattacharyya),

US Pub. No. 2004/0087084 to Hsieh (Hereinafter: Hsieh),

US Pub. No. 2004/0094763 to Agnello et al. (Hereinafter: Agnello), and/or  
US Pub. No. 2004/0018668 to Maszara (Hereinafter: Maszara).

24. **Huang teaches** substantially all of the limitations as stated above, but **Huang does not explicitly teach** the IC comprising silicon-on-insulator.
25. **Bhattacharyya discloses** an IC comprising silicon-on-insulator (Abstract; ¶4, 15), **Hsieh discloses** an IC comprising silicon-on-insulator (¶24), **Agnello discloses** an IC comprising silicon-on-insulator (¶49), and **Maszara discloses** an IC comprising silicon-on-insulator (¶2).
26. It would have been obvious to one of ordinary skill in the art at the time of the Applicant's invention to have combined the teachings of Huang with one or more of Bhattacharyya, Hsieh, Agnello, and/or Maszara to utilize an IC comprising silicon-on-insulator in order to:
- provide advantages of significant speed, power, and radiation immunity (Bhattacharyya: ¶4);
  - reduce undesired capacitance (Maszara: ¶2),
  - suppress short channel effect (Maszara: ¶2),
  - reduce latch-up and soft errors (Maszara: ¶2), and/or
  - implement well-documented (Maszara: ¶2), well-known (Hsieh: ¶ 24), and conventionally utilized (Bhattacharyya: Abstract; ¶15; Agnello: ¶49) SOI technology.

#### ***Response to Arguments***

27. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SURESH MEMULA whose telephone number is (571)272-8046. The examiner can normally be reached on Monday-Friday 8:00-4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suresh Memula/

Art Unit 2825  
October 22, 2008

/Phallaka Kik/  
Primary Examiner, Art Unit 2825